CLAIMS:

1. A dual residue pipelined AD-converter for converting an analog input signal to a digital output signal, said converter comprising a cascade of dual residue converter stages (S_1 ... S_N), the first of said stages (S_1) comprising means to receive the analog input signal (I), means (G_1) to derive one or more digital bits (D_1) from said analog input signal and means (H_1) to generate first and second residue signals (A_1, B_1) representing the quantization error left after the AD-conversion of said first stage, each of the following stages (S_2 ... S_N) in the cascade of dual residue converter stages comprising means to receive the first and second residue signals (A_1 ... A_{N-1}, B_1 ... B_{N-1}) generated by the previous stage in the cascade, means (G_2 ... G_N) to derive one or more further digital bits (D_2 ... D_N) from said received first and second residue signals and each of said following stages except the last one in the cascade comprising means (H_1 ... H_{N-1}) to generate first and second residue signals (A_2 ... A_{N-1}, B_2 ... B_{N-1}) representing the quantization error left after the AD-conversion of the stage, characterized in that each of the stages (S_1 ... S_{N-1}) of the dual residue pipelined AD-converter, except the last one, comprises switched capacitor means for the generation of the first and second residue signals (A_1 ... A_{N-1}, B_1 ... B_{N-1}).

2. A dual residue pipelined AD-converter as claimed in claim 1 characterized in that each of said following stages except the last one comprise input capacitors (C_3 ... C6) for receiving during a sampling phase the first and second residue signals generated by the previous stage, switching means (φ)to transfer during a tracking phase the charge of said input capacitors to first and second output capacitors (C'_3, C'_4), and means to generate first and second residue signals (A_2, B_2) from said first and second output capacitors (C'_3, C'_4) respectively.

3. A dual residue pipelined AD-converter as claimed in claim 2 characterized in that said switching means (φ) are arranged to transfer charge from said first received residue signal (A_1) to said first output capacitor (C'_3) with a gain factor of approximately 2 and charge from both said first (A_1) and second (B_1) received residue signals to said second output capacitor (C'_4) each with a gain factor of approximately 1 in a first sub-range mode

($D_2 = 0$) and to transfer charge from said second received residue signal (B_1) to said second output capacitor (C'_4) with a gain factor of approximately 2 and charge from both said first (A_1) and second (B_1) received residue signals to said first output capacitor (C'_3) each with a gain factor of approximately 1 in a second sub-range mode ($D_2 = 1$).

4. A dual residue pipelined AD-converter as claimed in claim 3 characterized in that said switching means are additionally arranged to transfer charge from both said first (A_{1+}, A_{1-}) and second (B_{1+}, B_{1-}) received residue signals to said first output capacitor ($2C'_{17}$) with a gain factor of approximately 3/2 and 1/2 respectively and charge from both said first (A_{1+}, A_{1-}) and second (B_{1+}, B_{1-}) received residue signals to said second output capacitor ($2C'_{18}$) with a gain factor of approximately 1/2 and 3/2 respectively in a third sub- range mode ($E = 1$) which lies symmetrically between said first and second sub-range modes.

5. A dual residue pipelined AD-converter as claimed in claim 2 characterized in that for the generation of each residue signal (A_2, B_2) an operational amplifier (J_3, J_4) is provided and that each output capacitor (C'_3, C'_4) is connected during the tracking phase (φ) between an output terminal and the inverting input terminal of said operational amplifier.

6. A dual residue pipelined AD-converter as claimed in claim 5 characterized in that one side of each input capacitor ($2C_{19}$ ... C_{30}) is connected to said inverting input terminal both during the sampling phase (φ) and during the tracking phase (φ) and that each output capacitor (C'_{13} ... C'_{16}) is charged during the sampling phase by the offset voltage at the inverting input of the operational amplifier (J_9, J_{10}).

7. A dual residue pipelined AD-converter as claimed in any of the preceding claims, characterized in that in that the switched capacitor means are arranged to receive balanced first and second residue signals (A_{1+}, A_{1-}, B_{1+}, B_{1-}) and to generate there from balanced first and second residue signals (A2+, A_{2-}, B_{2+}, B_{2-}) for application to the next stage in the cascade.